Low Complexity Finite Control Set Model Predictive Control for Neutral-Point Clamped Converters with Switching Constraints

Dimas A. Schuetz\textsuperscript{1}, Fernanda Carnielutti\textsuperscript{1}, Mokhtar Aly\textsuperscript{2}, Margarita Norambuena\textsuperscript{3}, José Rodriguez\textsuperscript{2}, Humberto Pinheiro\textsuperscript{1}

\textsuperscript{1}Federal University of Santa Maria (UFSM), Santa Maria, Brazil
\textsuperscript{2}Facultad de Ingeniería, Arquitectura y Diseño, Universidad San Sebastián, Bellavista 7, Santiago 8420542, Chile
\textsuperscript{3}Electronics Engineering Department, Universidad Tecnica Federico Santa Maria, Valparaíso, Chile

\texttt{dimasschuetz@gmail.com, fernanda.carnielutti@gmail.com, mokhtar.aly@uss.cl, margarita.norambuena@usm.cl, jose.rodriguezhp@uss.cl, humberto.cltab.ufsm.br@gmail.com}

Abstract—In this paper, a fast Finite Control Set Model Predictive Control algorithm is proposed for a three-phase grid-tied Neutral-Point Clamped converter. The system model is represented in the converter line-to-line voltages, where the voltage vectors assume only integer entries. First, the unconstrained voltage vector is obtained to minimize the current tracking error. Then, ellipse constraints are considered in the resulting Space-Vector diagram to limit the converter transitions between only adjacent levels in the phase voltages, aiming to ensure safe commutations of the power converter semiconductor devices. As a result, the constrained voltage vector can be rounded to the nearest converter vector, which should be implemented in the next sampling period. In addition, from the redundencies of the selected vector, a cost function is evaluated to ensure the neutral point current control, aiming to balance the dc-link capacitor voltages. As both control objectives are treated in a cascaded sequence, the proposed algorithm avoids the design of weighting factors and has the advantages of low computation burden, fast transient response, and good steady-state performance. Real-time Hardware-in-the-Loop results show the good performance of the proposed algorithm compared to other techniques with reduced computational burden.

Index Terms—Cost Function, Finite Control Set Model Predictive Control, Grid-Tied Inverters, Multilevel Converters.

I. INTRODUCTION

FINITE Control Set Model Predictive Control (FCS-MPC) is considered an interesting alternative for multilevel converter due to its advantages when compared to classical control techniques, such as easy inclusion of constraints, multiple variable control, and combination of control and modulation stages in the same algorithm [1]. Recently, FCS-MPC algorithms have been proposed for different voltage-fed multilevel converters topologies, such as Neutral-Point Clamped (NPC), Flying Capacitor (FC), Active NPC (ANPC), Split Source Inverter (SSI), Modular Multilevel Converter (MMC), and many others [2]–[6]. Usually, the complexity of the FCS-MPC algorithm depends on the converter number of levels and prediction horizon, requiring digital processors with high computational capacity for online calculations, especially for multilevel converters with a high number of levels.

In order to reduce the number of calculations of the FCS-MPC algorithms, different ways of solving the optimization problem were proposed in the literature, such as the division of the complete optimization problem into smaller ones, implementation of the Sphere Decoding Algorithm (SDA), as well as by dynamic programming and greedy algorithms [7]–[9]. In [10], a Cascaded FCS-MPC algorithm is proposed where the optimization problem is divided into two different cascaded FCS-MPCs: minimization of the current tracking error and balance of the capacitor voltages, avoiding the requirement of weighting factors design. Alternatively, in [11], an improved and simplified branch-and-bound algorithm was presented to reduce the execution time of the FCS-MPC algorithm. Although the computational burden is reduced by these algorithms, the computational time still increases with the increase in the number of converter voltage levels.

Instead of calculating the cost function for all converter voltage vectors, some authors have proposed to limit the search for the next candidate voltage vector, in order to reduce the number of calculations for the FCS-MPC algorithm [12], [13]. To do that, the distance between the reference vector and the converter voltage vectors is calculated, and the nearest vector is selected to be implemented in the next sampling period. Moreover, the inclusion of different control variables in the same cost function requires the accurate design of the weighting factors, which is a well-known challenge in the FCS-MPC algorithm and has a direct impact on the performance of the controlled variables [14].

This paper presents a fast FCS-MPC algorithm for a three-phase grid-tied NPC inverter with an LCL filter. The system model and the NPC voltage vectors are represented in the line-to-line voltage coordinate system, as integer entries, where the unconstrained voltage reference from the current

This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brasil (CAPES/PROEX) – Finance Code 001, in part by the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), in part by Fundação de Amparo à Pesquisa do Estado do RS (FAPERGS), in part by ANID through projects SERC Chile (ANID/FONDAP15110019), AC3E (ANID/Basal/FB0008), FONDECYT 11180233, ACT192013, 1210208 and 1230250.
control can be obtained in a fast way [15]. In addition, the constraints of adjacent switching transitions and feasibility are included, limiting the search space to a two-level SV diagram, where the nearest voltage vector is obtained by rounding the constrained reference, without the need for multiple cost function evaluations and weighing factors design. Considering a common-mode voltage limitation criteria, a set of redundant phase-voltage vectors is defined with transitions only between adjacent vectors, and a cost function is evaluated to find the optimal redundancy to balance the dc-link capacitor voltages. As a result, the Fast FCS-MPC algorithm presents a low computational burden and results in output voltage with limited $dv/dt$ over the output filter, fast transient response, and good steady-state performance, as well as can be easily expanded to other multilevel topologies without loss of generality.

This paper is organized as follows: Section II presents the system model of the grid-tied NPC converter in the line-to-line voltage coordinates; Section III describes the proposed Fast FCS-MPC algorithm with the inverter constraints and control of the neutral-point current; and in Section IV, Hardware-in-the-Loop (HIL) real-time results of the proposed algorithm and comparisons are presented. Finally, Section V summarizes the main conclusions of the paper.

II. SYSTEM MODEL IN THE LINE-TO-LINE VOLTAGES COORDINATE SYSTEM

This section describes the proposed Fast FCS-MPC algorithm, assuming a three-phase grid-tied NPC inverter with an LCL filter. The complete system is represented in Fig. 1.

A. Operation Principle of the NPC Inverter

The NPC inverter is usually employed in grid-tied applications due to its advantages when compared to the conventional two-level inverter, such as higher number of levels in the output voltages and lower reverse blocking voltages across the semiconductor devices, making it suitable for medium- and high-power applications [16]. Table I presents the possible switching states for each phase of the NPC inverter.

In the NPC topology, each phase voltage can be synthesized by a unique switching state combination. On the other hand, some line-to-line voltage levels can be generated by different phase-voltage combinations, which result in different current polarities in the neutral point of the dc-link. Usually, under normal operation conditions, the voltage across the NPC semiconductor switches is limited to half the value of the dc-link voltage. However, due to some non-idealities, such as dead-time, parasitic capacitances, and inductances, the internal switches ($S_{2x}$ and $S_{3x}$) can be submitted up to the total dc-link voltage [17]. In order to prevent this over-voltage across $S_{2x}$ and $S_{3x}$, the transition between states “-1” to “1”, and vice-versa, should be avoided to ensure the safe operation of the NPC inverter [18].

B. Simplified System Model

In this paper, the system presented in Fig. 1 is modeled in a simplified way, where the LCL filter is approximated by an L filter and the filter capacitor voltages are considered as disturbances, as proposed in [19]. As a result, only the inverter-side currents and filter capacitor voltages need to be measured, allowing a reduction in the number of sensors for the system. It is important to highlight that the simplified formulation adopts a passive damping strategy by incorporating damping resistors in series with the filter capacitors, aiming to reduce the effects of the LCL filter resonance.

By applying Kirchhoff’s Voltage Law (KVL) in the inverter-side of the LCL filter, it is possible to write:

$$-u_{an} + L_1 \frac{di_{a1}}{dt} + v_{Ca} - v_{Cb} - L_1 \frac{di_{b1}}{dt} + u_{bn} = 0$$

$$-u_{bn} + L_1 \frac{di_{b1}}{dt} + v_{Cb} - v_{Cc} - L_1 \frac{di_{c1}}{dt} + u_{cn} = 0,$$

where $u_{an}$, $u_{bn}$ and $u_{cn}$ represent the NPC output phase-voltages, $v_{Ca}$, $v_{Cb}$ and $v_{Cc}$ are the LCL filter capacitor voltages, $i_{a1}$, $i_{b1}$ and $i_{c1}$ are the inverter-side currents and $L_1$ is the inverter-side filter inductance. From (1), it is possible to represent the dynamic equations of the system by their line-to-line quantities, which results in:

$$L_1 \frac{d}{dt}(i_{ab1}) = -v_{Cab} + u_{ab}$$

$$L_1 \frac{d}{dt}(i_{bc1}) = -v_{Cbc} + u_{bc},$$

where $i_{ab1}$ and $i_{bc1}$ can be interpreted as the inverter-side line-to-line currents, $v_{Cab}$ and $v_{Cbc}$ are the line-to-line filter capacitor voltages and $u_{ab}$ and $u_{bc}$ are the line-to-line inverter output voltages. As a result, without loss of generality, it is possible to represent the output inverter vectors in a two-dimensional coordinate system [20]. Fig. 2 shows the SV diagram for the three-phase NPC inverter, represented in the output line-to-line voltages coordinate system and normalized.

![Fig. 1. Three-phase grid-tied NPC inverter with LCL filter.](image-url)
to half the value of the dc-link voltage, with integer voltage vectors [15].

In order to obtain the discrete-time system equations, a fixed small sampling period $T_s$ is assumed and the Euler method is applied to (2), resulting in:

$$i_{ab1}(k+1) = i_{ab1}(k) + \frac{T_s}{L_1}u_{ab}(k) - \frac{T_s}{L_1}v_{Cab}(k)$$

$$i_{bc1}(k+1) = i_{bc1}(k) + \frac{T_s}{L_1}u_{bc}(k) - \frac{T_s}{L_1}v_{Cbc}(k),$$

which are also represented in the output line-to-line voltage coordinate system.

### III. Proposed Fast FCS-MPC Algorithm

Beginning from the assumption that the inverter-side currents $i_1$ will properly track their reference values $i_1^*$ for each sampling period, let us consider:

$$i_{ab1}(k+2) = i_{ab1}(k+2)^*$$

$$i_{bc1}(k+2) = i_{bc1}(k+2)^*$$

where the notation $k+2$ considers the implementation delay of the microprocessor.

From (3) and (4), the inverter unconstrained output voltages references to achieve the current references in the next sampling period, expressed in the line-to-line voltages coordinates, can be determined as:

$$u_{ab}^*(k+1) = \frac{L_1}{T_s} \left( i_{ab1}(k+2)^* - i_{ab1}(k+1) \right) + v_{Cab}(k+1)$$

$$u_{bc}^*(k+1) = \frac{L_1}{T_s} \left( i_{bc1}(k+2)^* - i_{bc1}(k+1) \right) + v_{Cbc}(k+1).$$

#### A. Constrained Solution

In this paper, the unconstrained reference vector $u_1^*(k+1)$ is limited in order to guarantee its feasibility and the proper voltage clamping of the NPC inverter. In order to simplify the implementation, ellipses on the SV diagram are proposed to constrain the region for the reference voltage vector in the SV diagram. Fig. 3 shows the two constraints adopted in this paper.

First, the reference vector should be constrained to the region where the switching vectors present at least one redundancy which has at most a one-level transition in each inverter phase voltage. This is achieved by centering the blue ellipse of Fig. 3, around the last implemented line-to-line voltage vector. As a result, the voltage clamping of the internal switches of the NPC legs is ensured. In the sequence, the reference voltage vector is constrained by the black one, in order to result in a region where only feasible inverter voltage vectors can be selected from it.

The quadratic equation of the ellipse is given by:

$$u_{ab}^2 + u_{ab}u_{bc} + u_{bc}^2 = c. \quad (6)$$

Initially, a coordinate translation is carried out, where the origin of a new line-to-line coordinate system is set at the last implemented line-to-line voltage vector $u(k)$, such as:

$$u_{ab}^* = u_{ab}(k+1) - u_{ab}(k)$$

$$u_{bc}^* = u_{bc}(k+1) - u_{bc}(k). \quad (7)$$

Then, the unconstrained vector is limited by the first ellipse constraint (blue curve), which can be done by solving (6) for the unconstrained vector in the new coordinate system:

$$u_{ab}^2 + u_{ab}u_{bc}^* + u_{bc}^* = c_1(k+1). \quad (8)$$

where $c_1(k+1)$ is computed at every sampling instant for a given voltage reference. If $c_1(k+1)$ is larger than $F_1$, which defines the maximum size of the ellipse that results in at most one transition in the phase voltages, then the reference vector is limited as:

$$u_{ab}^*(k+1) = \frac{F_1}{c_1(k+1)}$$

$$u_{bc}^*(k+1) = \frac{F_1}{c_1(k+1)}, \quad (9)$$

where $F_1 = \frac{3}{16}V_{bc}^2$. So, the limited SV space corresponds to a two-level inverter SV diagram around $u(k)$, where at least one redundancy meets the switching transitions constraint.

In the sequence, the constrained reference vector is remapped to the original line-to-line coordinate system ($u_{ab}$, $u_{bc}$), where the second constraint (black curve) is evaluated.
in order to guarantee that the reference vector lies inside the maximum feasible region. It is given by:

\[ u_{ab}(k+1) = \sum_{\text{adjacent}} F_2 \sum_{\text{adjacent}} c_2(k+1). \]  

(10)

If \( c_2 \) is larger than the maximum ellipse length for the feasible vectors \( F_2 \), the reference vector is limited as:

\[ u_{ab}(k+1) = \sum_{\text{adjacent}} F_2 \sum_{\text{adjacent}} c_2(k+1), \]  

(11)

where \( F_2 = \frac{13}{10} V_{dc}^2 \).

A fast way to obtain the inverter voltage vector to be implemented is by rounding the reference vector such as:

\[ \begin{bmatrix} u_{ab}(k+1) \\ u_{bc}(k+1) \end{bmatrix} = \text{round} \left( \begin{bmatrix} u^*_{ab}(k+1) \\ u^*_{bc}(k+1) \end{bmatrix} \right), \]  

(12)

where the resultant voltage vector, in the line-to-line voltage coordinates, contains at least one redundancy that presents at most one phase-voltage level transition. It can be noted that, with the projection of the unconstrained solution over the ellipses constraints, the chosen vector may be a sub-optimal solution, according to the operational point of the system.

Note that some vectors represented in Fig. 2 have more than one switching states combination which results in the same line-to-line voltages, which are called redundancies. To select a specific redundant vector in the phase-voltage space, a common-mode voltage criterion helps to check that at most one level change occurs per phase. It computes the common-mode voltage difference \( \Delta v_o \) from the last implemented vector \( u^{(k)} \) to the candidate redundancies of the selected vector \( u^*(k+1) \) as:

\[ \Delta v_o = v_o(u^{(k)}) - v_o(u^*(k+1)), \]  

(13)

where \( v_o(u^{(k)}) \) is the common-mode voltage of the last implemented vector and \( v_o(u^*(k+1)) \) refers to the common-mode voltage of the candidate redundancy.

Considering an SV diagram of a two-level three-phase inverter, where each phase voltage commutates at most one level, the common mode voltage difference of two voltage vectors is less or equal to 2, i.e., \( |\Delta v_o| \leq 2 \). By expanding this criterion to a three-level SV diagram, the redundancies that satisfy it are selected as the set of candidate vectors \( \Omega u_{abc(k+1)} \) to be implemented in the next sampling period. Note that the constrained algorithm can be easily expanded to other topologies to avoid phase transitions between two adjacent levels, which increases the switching losses of the converter and the \( dv/dt \) across the output filters.

\section*{B. Cost Function for Neutral-Point Balance}

Once the redundancies of the chosen inverter voltage vector are defined, a cost function composed of the capacitor voltage error is defined in order to choose which redundancy to implement in the next sampling period:

\[ J = \left( \frac{V_{dc}}{2} - v_{c1}(k+2) \right)^2, \]  

(14)

where \( v_{c1(k+2)} \) is the predicted voltage over the upper dc link capacitor \( C_1 \) at \( (k + 2) \), which can be estimated from:

\[ v_{c1(k+2)} = v_{c1(k+1)} + \frac{T_s}{C_1} i_{c1(k+1)}, \]  

(15)

where \( i_{c1(k+1)} \) is the predicted current that will flow through \( C_1 \). It can be estimated from the equation of the current that flows into the neutral point, that is:

\[ i_{n(k+1)} = \sum_x i_{x1(k+1)} \left( 1 - 2 \left| \frac{u_{xn(k+1)}}{V_{dc}} \right| \right), \]  

(16)

where \( x \in \{a, b, c\} \) indicates the corresponding inverter phase and \( 2 \frac{u_{xn}}{V_{dc}} \in \{-1, 0, 1\} \) is the candidate inverter phase voltage to be implemented.

Assuming that the total dc-link voltage is constant or varies slowly in time, we have:

\[ i_{c1(k+1)} = \sum_x i_{x1(k+1)} \left( \frac{1}{2} - \left| \frac{u_{xn(k+1)}}{V_{dc}} \right| \right). \]  

(17)

Since we are addressing a three-phase three-wire system, (17) can be simplified to:

\[ i_{c1(k+1)} = -\sum_x i_{x1(k+1)} \left| \frac{u_{xn(k+1)}}{V_{dc}} \right|. \]  

(18)

It is possible to obtain the feasible converter phase voltage vectors by mapping the constrained optimum line-to-line voltage vector into the inverter phase space. This results in the one, two, or three inverter phase voltage vectors, \( \frac{V_{dc}}{2} \left[ u_{an}, u_{bn}, u_{cn} \right]^T \), for the considered NPC inverter. Now, the phase voltage vector to be implemented at \( (k + 2) \) is the one that results in the smallest cost function (14).

\section*{IV. HARDWARE-IN-THE-LOOP RESULTS}

This section presents different case study results of the proposed algorithm and comparisons with other FCS-MPC strategies, presented in the literature. To do this, high-fidelity real-time Hardware-in-the-Loop results were obtained and the algorithms are implemented in a well-known off-the-shelf digital signal processor, model TMS320F28335. The HIL test bed used is presented in Fig. 4 and Table II presents the main system parameters.

Initially, the performance of the proposed FCS-MPC algorithm is illustrated in Fig. 5. Fig. 5(a) shows two of the grid-injected currents and two line-to-line converter-side PWM voltages. In sequence, Fig. 5(b) presents the output converter phase voltages, which commutates only between adjacent levels, as expected by the minor ellipse constraint of the proposed algorithm. Moreover, Fig. 5(c) shows two inverter-side currents, and the dc-link capacitor voltages, indicating the voltage balance to the half value of the dc source.

In the sequence, a parameter-varying test is developed in order to evaluate the performance of the proposed algorithm under parameter uncertainties. To evaluate the performance of the proposed algorithm, the grid-side current Root-Mean-Square Error (RMSE), is considered, which is here calculated by:

\[ \text{RMSE} = \sqrt{\frac{1}{n_x \sum_{k=0}^{n_x} (i_x^2(k) - i_x(k))^2}} \]  

(19)
Table II

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid voltage</td>
<td>( v_{\text{g}} )</td>
<td>127/220 V @60 Hz</td>
</tr>
<tr>
<td>Fundamental Frequency</td>
<td>( f )</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Grid impedance</td>
<td>( Z_g )</td>
<td>( L_g = 1 \ \mu \text{H}, R_g = 0.1 \ \text{m\Omega} )</td>
</tr>
<tr>
<td>Rated power</td>
<td>( P_{\text{out}} )</td>
<td>27 kVA</td>
</tr>
<tr>
<td>dc bus voltage</td>
<td>( V_{\text{dc}} )</td>
<td>400 V</td>
</tr>
<tr>
<td>dc bus capacitance</td>
<td>( C )</td>
<td>4700 ( \mu \text{F} )</td>
</tr>
<tr>
<td>Inverter-side filter inductance</td>
<td>( L_1 )</td>
<td>900 ( \mu \text{H} )</td>
</tr>
<tr>
<td>LCL filter capacitance</td>
<td>( C_f )</td>
<td>100 ( \mu \text{F} )</td>
</tr>
<tr>
<td>Damping resistance</td>
<td>( R_d )</td>
<td>1 ( \Omega )</td>
</tr>
<tr>
<td>Grid-side filter inductance</td>
<td>( L_2 )</td>
<td>100 ( \mu \text{H} )</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>( f_s )</td>
<td>20 kHz</td>
</tr>
</tbody>
</table>

where \( n_s \) is the number of samples in one cycle of the fundamental frequency, \( i_2 \) is the grid-side current reference, and \( i_2 \) means the measured grid injected current.

Fig 6(a) shows the grid-side currents for a reduction of 33% in the inverter-side inductance (\( L_1 = 600 \ \mu \text{H} \)). In this case, the RMSE results in 2.6 A, and the current THD is equal to 4%. In addition, Fig 6(b) presents the same results for a change in the grid-side inductance parameters, which are assumed \( L_2 = 50 \ \mu \text{H} \), and \( L_g = 1 \ \text{mH} \). In this case, the RMSE and THD result in 2 A and 2.8 %, respectively. Finally, in Fig. 6(c) the grid-side currents are presented considering a parameter variation for \( L_1, L_2 \) and \( L_g \), resulting in 2.1 A for the RMSE and THD equal to 3.2 %.

In order to evaluate the performance of dc-link capacitor voltage balance, a test is evaluated considering the capacitor voltages unbalanced for different power factors (PF). Here, the capacitor voltages offset \( v_{\text{cf}} \) is considered, computed by:

\[
 v_{\text{cf}}(\%) = 100 \left( \frac{V_{\text{cc}}/2 - \bar{v}_{\text{a1}}}{V_{\text{cc}}/2} \right) 
\]

where \( \bar{v}_{\text{a1}} \) is the mean value of the measured half dc link voltage.

Fig. 7 shows the dc-link capacitor voltages, initially unbalanced, for two different power factors (PF), PF=1 in Fig. 7(a) and PF=0.7 in Fig. 7(b). As presented, when the test starts, the dc-link capacitor voltages are quickly balanced to their reference value, indicating the effectiveness of the cost function adopted in the proposed algorithm. Although it can be noted the presence of high-frequency ripple for the capacitor voltages with PF=0.7, they remain balanced to their reference values with similar \( v_{\text{cf}} \) as the case with PF=1, which are 0.24% and 0.16%, respectively.

In order to compare the performance of the proposed Fast FCS-MPC with similar approaches, a Branch and Bound FCS-MPC [11] and a Cascaded FCS-MPC [10] algorithms were selected and implemented in the HIL device for the grid-tied NPC inverter, with the same system parameters. The Branch and Bound FCS-MPC algorithm was proposed in [11] aiming to reduce the computational burden of the classical FCS-MPC algorithms. In this approach, the optimization problem is reduced to a two-variable integer quadratic programming problem, where the global optimal solution is evaluated from
an algorithm with a low computational burden. In [10] a Cascaded FCS-MPC is presented, where the cost function is divided and firstly evaluated to find the optimal vector that reduces the current tracking error. In sequence, from the selected optimal vector, the redundancies are evaluated to balance the neutral point. When compared to the classical FCS-MPC algorithm, the number of calculations for the cost function is minimized from 27 to 19 for an NPC inverter, which reduces the computational burden of the algorithm.

For the evaluation of the dynamic performance of these algorithms, Fig. 8 shows two grid-side currents and two inverter output line-to-line voltages for a step change in the current reference from 0 to 100 A. As presented, it is possible to note the similarity of the three algorithms, where a fast transient response is obtained. In addition, a steady-state comparison is presented in Table III in terms of computational burden, grid-side current THD, and capacitor voltage offset.

As presented in Table III, the proposed Fast FCS-MPC presents the lowest execution time, once the inverter voltage vector can be chosen directly from the rounding of the voltage reference; on the other hand, the cost function evaluation is required 19 times for the Cascaded FCS-MPC and 5 times for the Branch and Bound algorithm. Moreover, the three FCS-MPC algorithms present similar performances in terms of current THD and RMSE and capacitor voltage offset, highlighting the advantages of the Fast FCS-MPC algorithm, which presents a similar performance to optimal FCS-MPC algorithms with a lower computational burden.

<table>
<thead>
<tr>
<th>FCS-MPC Algorithm</th>
<th>Execution Time (μs)</th>
<th>Current THD (A)</th>
<th>Current RMSE (%)</th>
<th>Capacitor Voltage Fluc. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed FAST</td>
<td>5.34</td>
<td>2.91</td>
<td>1.98</td>
<td>0.38</td>
</tr>
<tr>
<td>Cascaded</td>
<td>15.2</td>
<td>2.37</td>
<td>1.40</td>
<td>0.36</td>
</tr>
<tr>
<td>Branch and Bound</td>
<td>8.81</td>
<td>2.75</td>
<td>3.75</td>
<td>0.38</td>
</tr>
</tbody>
</table>

Fig. 6. Inverter-side currents for LCL filter parameter varying. Horizontal scale: 4 ms/div.. Vertical: 50 A/div..
is verified by the measurement of the DSP execution time. Moreover, although the proposed algorithm can result in a sub-optimal solution and can limit the transient performance due to the switching constraint, comparison results indicate a similar performance in terms of grid-currents THD tracking error, and capacitor voltage fluctuation.

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V. CONCLUSIONS

This paper presented a Fast FCS-MPC algorithm, formulated in the output line-to-line voltage coordinates, where the inverter voltage vectors are represented with only integer entries. The inverter voltage vector to be implemented can be obtained by rounding the reference vector, which includes the feasibility and converter switching constraints. Once the inverter voltage vector is defined, its redundancies are generated from a common-mode voltage constraint criteria, which ensures that the converter switches between only adjacent vectors, reducing the $dv/dt$ of the output voltages. A cost function is evaluated for the set of redundant vectors to balance the dc-link capacitor voltages. It is important to notice that the cost function can be evaluated at most two times, significantly reducing the computational burden of the algorithm, which