Design Improvement of Self-Oscillating Resonant Converters Accounting for Gate Charge in High-Frequency LED Drivers

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***Abstract*—Increasing the operation frequency of Self-Oscillating Resonant Converters (SORC) is a challenge due to reasons such as higher switching, magnetic component and driving circuit losses, but mainly due to the effects of the parasitic components of the switching devices and their impact on the precision between the operating and designed frequencies of the converters. This paper evaluates, both in SPICE and experimentally, two SORC models and design methodologies at frequencies higher than they were traditionally designed to operate, with the purpose of finding which constraints of such methodologies determine the frequency ceiling, i.e., the maximum achievable self-oscillating frequency of the converter as well as the deviation from the designed frequency when comparing traditional and improved methodologies. An improved design equation which considers the required gate-charge for the gate of the converter switching device is also considered as a condition for a sustained self-oscillation operation in higher frequencies, expanding the methodologies original frequency limitation.**

***Index Terms*—Self-Oscillating, LED lighting, resonant converter, frequency enhancement**

I. Introduction

Despite the widespread utilization of the Self-Oscillating Resonant Converters (SORC) in discharge lamp ballasts due to their low component number, high-reliability and cost-effectiveness [1]–[3], as LEDs replaced discharge lamps in most lighting applications, the industry predominantly adopted driver designs based on more versatile and easy-to-design dedicated integrated circuits [4], [5]. This shift can be partially attributed to the trend of operating lighting drivers at higher frequencies, ranging from hundreds of thousands of kHz [6] to the MHz range [7], in order to achieve smaller passive components. Traditional self-oscillating circuits design methodologies were only tested, implemented and validated for lighting in the range of dozens of kHz [8] up to few hundreds of kHz [9] and were not meant for higher frequency operation.

Nevertheless, academic researchers have continued to explore the application of SORCs as LED drivers [10]–[12], resulting in more advanced models [13], design methodologies [14] and the use of new switch topologies, like the GaNFET [15]. However, while there have been notable developments in the academic literature on self-oscillating circuits, comprehensive studies on the practical constraints of increasing the operating frequency of existing SORC topologies are lacking. In this paper, two methodologies for SORC design through the use of SPICE simulation and experimental testing are evaluated. Whilst the literature does present alternative methods [16], [17], the two evaluated methodologies [14], [18] use the Describing Function (DF) method to provide approximate results with a relatively simple sequence of steps that require simpler math.

Both methodologies are tested while the frequency is sequentially raised, from the conventional dozens of kHz they were originally designed to achieve, up to 1 MHz. As the operating frequency increases, the underlying assumptions within the design models lead to a perceived discrepancy between the design specifications and the practical outcomes. This disparity establishes a frequency ceiling for each methodology, beyond which additional parameters must be considered for the construction of a more comprehensive model. Such a model should account for the parasitic elements of the switching devices and their previously neglected dynamics.

In this paper, as a result of experimenting with the design parameters in simulation, a novel empirical condition for high-frequency self-oscillation was found, previously undocumented in the literature. This new parameter is related to the charge of the gate capacitance of the switches. By incorporating gate charge measurements into the design stage, greater self-oscillating range and design accuracy is achieved in simulation. These findings are subsequently experimentally validated in the paper.

II. The Self-Oscillating Resonant Topology

A resonant inverter typically consists of a DC bus voltage supplying power to an inverter stage, often an asymmetrical half-bridge or full-bridge converter. This inverter stage generates a square waveform that is then passed through a resonant filter stage, that attenuates harmonics of the applied square voltage, producing an almost sinusoidal current for the load with a frequency identical to resonance. For applications involving DC outputs, such as LED lighting, an additional stage becomes necessary at the output end. This supplementary stage typically includes a full-bridge rectifier and a filtering circuit as presented at Fig. 1. These components are crucial for ensuring that the output voltage remains stable and free from unwanted fluctuations, thus meeting the rigid requirements of LED lighting systems.

The choice of the resonant tank configuration allows for some design flexibility. Among common filter choices, like the LLC and the LCC, the LC series filter is commonly employed in resonant converters used for LED lighting due to its simplicity [19]. Operating with a switching frequency higher than the resonant frequency of the inverter results in a inductive characteristic that enables Zero Voltage Switching (ZVS), effectively reducing switching losses [19].

In the Self-Oscillating control circuit using MOSFETs, the almost sinusoidal current that flows in the resonant filter is reflected to the gates using a current or voltage transformer (CT or VT), depending on the SORC topology, with two zener-clamped (Z_{D1-4}) secondary windings (Fig. 2). This safely and efficiently drives the gates of the inverter switches.

A. Overview of SORC's Operation

The circuit depicted in Fig. 2 illustrates the primary elements of a SORC system, which includes an LC filter and an LED serving as the load. The startup circuit comprises three main components: R_1, C_1, and the diac D_2. When the bus voltage E is connected to R_1 and C_1, the voltage across C_1 gradually increases until it matches the breakdown voltage of the diac D_2. When this threshold is reached, the diac momentarily activates, generating a positive gate-to-source voltage V_{gs} on S_2.

During the initial stage of operation, after the startup phase, switch S_2 conducts and supplies current to L_F, C_F, the output rectifier, the load and L_{ct1}. As a result, switch S_2 remains with a positive gate-to-source voltage (V_{gs}), while switch S_1 has a negative V_{gs} and remains in the off-state due to the opposing polarity of L_{ct2} and L_{ct3}.

The second stage of operation starts when the current through the resonant circuit reaches zero and reverses polarity. As the current flows in the opposite direction, the three-winding current transformer (CT) induces a polarity change in the gate to source network. Additionally, the voltage source E is disconnected from the circuit, and the load is supplied by the resonant filter through switch S_2. The current gradually decreases until the end of this stage, causing L_{ct1} to apply a positive voltage to the gate of switch S_2, which resets the converter to the start of the first stage of operation.

III. SORC Design Methodology

The design of a SORC consists of two essential steps. First, the filter topology, which includes the passive power inductors and capacitors, is designed to create a resonant tank operating at a specific frequency. The choice of resonant frequency is critical for optimizing efficiency and power conversion [20]. Second, the self-oscillating control circuit (SOCC) is designed to regulate and control the SORC's operation.

A. LC Series Resonant Filter Design

Designing an LC series resonant filter involves selecting values for the inductance (L_F) and capacitance (C_F) components. For this paper, the bus voltage E is also considered as a variable design parameter. Although this is not required, it does expand the available solution space for the filter design. Fig. 3 presents the general resonant frequency characteristic of an LC filter, highlighting the desired operation point.

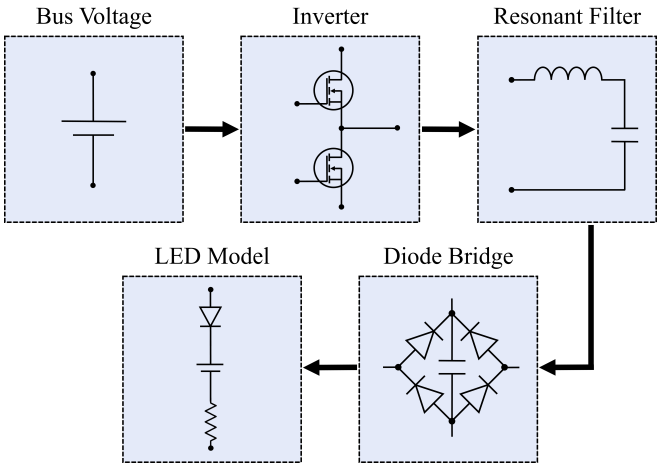

Fig. 1. Typical Half-Bridge LC resonant inverter structure.

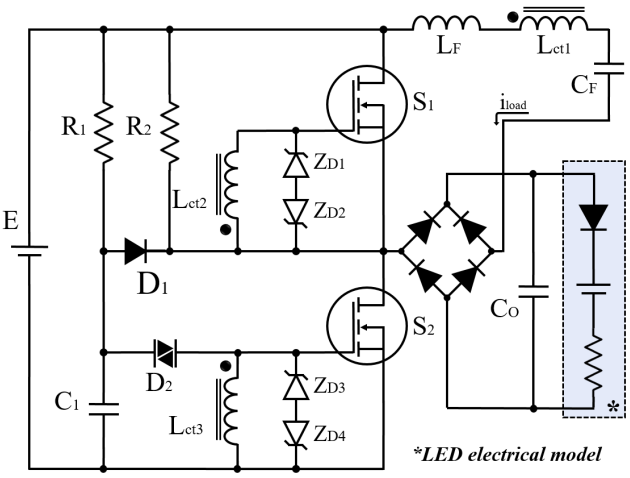

Fig. 2. Self-Oscillantig LC inverter for LED load.

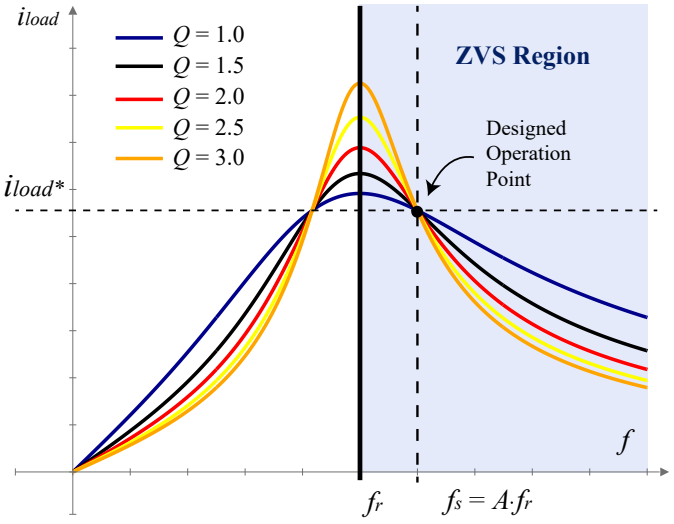

Fig. 3. Resonance characteristics of LC filter.

The values for L_F, C_F and E must be chosen such that the filter achieves four goals, related to our design parameters: Exhibits a resonance peak at a specific frequency f_r; does it with an appropriate quality factor Q; keeps the design load current i_{load}; and does it at the nominal switching frequency f_s; The load resistance R_{ac}, determined by the application, is a fixed parameter.

We choose an intended (f_r) for the filter based on realistic expectations for the availability of passive components values and switches. The resonant frequency is related to the components through (1).

$$f_r = \frac{1}{2\pi\sqrt{L_F \cdot C_F}} \tag{1}$$

The actual switching frequency f_s, however, does not need to match the resonant frequency f_r, but is rather given by (2). The choice of the normalized switching frequency A should account for the operation conditions: for the LC filter, choosing an A value above unity means that the ZVS condition should be achieved.

$$f_s = A \cdot f_r \tag{2}$$

Considering the equivalent resistance R_{ac} of the series circuit, the higher the quality factor (Q), the narrower the bandwidth around the resonant frequency. The quality factor of the resonant filter determines the sharpness of the resonance peak and can be determined by (3) .

$$Q = \frac{1}{R_{ac}}\sqrt{\frac{L_F}{C_F}} \tag{3}$$

For LED loads, with equivalent DC resistance R_{led}, an equivalent AC load resistance R_{ac} must be considered. By employing the rectifier and low-pass filter arrangement at the converter output, as presented in Fig. 2, R_{ac} can be determined through (4) [21].

$$R_{ac} = \frac{8}{\pi^2} R_{led} \tag{4}$$

With these equations, a closest fit routine is executed, which gives precise values for L_F, C_F, and E. With practical component values, it's not possible to perfectly achieve all characteristics at the same time, due to the non-idealities of the circuit. As accurate predictions of actual f_r and i_{load} are important for the design of the SOCC, it's recommended that the practical values are retrofitted into the resonant tank routine in order to minimize parameter error.

B. Self-Oscillating Command Circuit Design

Once the resonant filter parameters are defined, the resulting current, with its frequency f_s and amplitude i_{load} are considered as a current source input i_p/n, which is transferred through the CT to the command circuit, according to Fig. 4. The model includes not only the effects of the CT's inductance, but also the zener diodes and, possibly, the equivalent MOSFET gate capacitance.

1) First Methodolody: Part of the challenge of designing a SORC is the modelling of the intrinsic non-linear characteristic of the command circuit. The methodology presented by [18] utilizes the aforementioned DF (Fig. 5) to model the switching characteristic and the extended Nyquist stability criterion, which assesses the presence of self-sustained oscillation and ensures the stability of the analyzed system.

To determine the magnetizing inductance L_m of the SOCC referred to the secondary of the CT, one must first establish the appropriate turns ratio (n) by considering primary and secondary currents (i_z and i_p). It's likely that n is not an exact number, but rather the practical square relationship bewtween primary and secondary inductances. This value must be chosen so that, in the secondary winding of the current transformer, there is enough current to bias the Zener diodes i_z. The gate current i_g is not considered for now. In [11], [13]–[15], [18] the current transformer n value is determined by (5).

$$n = 2\frac{i_x}{i_p} = 2\frac{i_z}{i_p} = 2\frac{P_z}{V_z}\frac{1}{i_p} \tag{5}$$

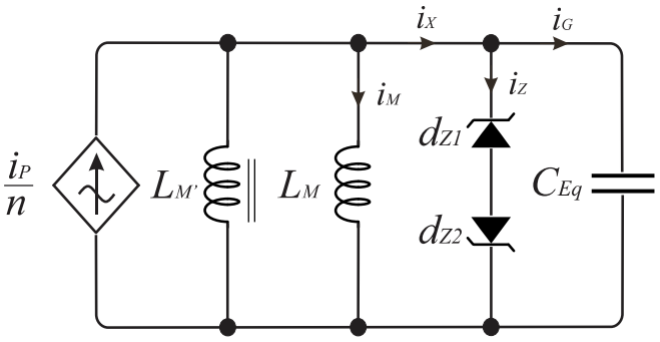

Fig. 4. Self-oscillating control circuit model, presented in [14].

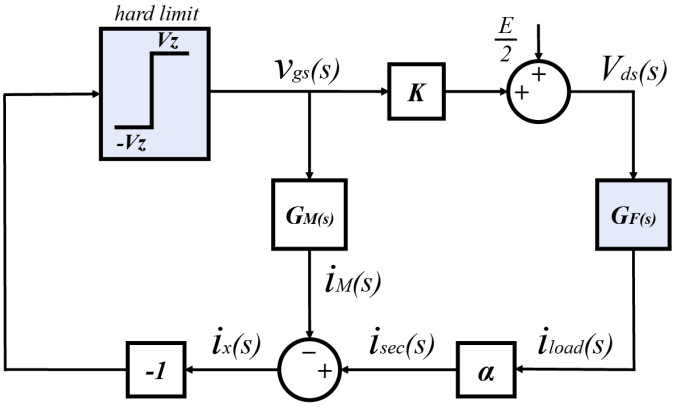

Fig. 5. Describing Function (DF) for a Self-Oscillating Resonant Converter.

The power P_z and voltage V_z are design inputs for each of the zener diodes on the SOCC. The zener diode breakdown voltage V_z is chosen to match a safe and efficient level to drive the chosen switches. The zener's power P_z should be chosen so that, at nominal current, it consumes half of the maximum dissipation of the chosen semiconductor package.

As the secondary voltage is approximated by a square voltage with peak value V_z, the gain K (6) in the describing function relates the secondary zener clamped square voltage and the primary V_{ds} square voltage with amplitude E.

$$K = \frac{E}{2V_z} \tag{6}$$

The equivalent gain of the resonant filter is given by the inverse of the filter's impedance (7). The imaginary part β of the filter gain - related to steady-state conditions - is given by (8).

$$G_f = \frac{1}{Z_f} \tag{7}$$

$$\beta(j\omega) = Im(G_f) \tag{8}$$

Therefore, the desired magnetizing inductance L_m is calculated using (9) and this value is reflected to the primary using (10).

$$L_m = \frac{-1}{K.\alpha.\omega.\beta(j\omega)} \tag{9}$$

$$L_{pri} = L_m \left(\frac{1}{n}\right)^2 \tag{10}$$

2) Second Methodology: The accuracy of the methodology is further increased in [13] and [11], both papers that expand the frequency range of the converter by compensating for the behaviour of the parasitic gate capacitance of the MOSFET switch. In [11], the DF is adjusted to account for C_{Eq} and, in [13], not only the capacitance value is considered in the closed-loop diagram, but also the trapezoidal characteristic of the sinusoidal current that is cut-off by the zener diodes. However, the secondary current i_x is calculated in the same way as in the first methodology. Equation (11) introduces a new variable $\beta'(j\omega)$, which is found as a function[1] of parameters i_x, ω, C_{Eq} and V_z.

$$\beta'(j\omega) = f(i_x, \omega, C_{Eq}, V_z) \tag{11}$$

The inclusion of this new variable β', which considers C_{Eq}, substantially modifies the values of the resulting magnetizing inductance L_m and, therefore, the secondary inductance of the CT (12). The reflected inductance of the primary of CT L_{pri} is also calculated using (10).

$$L'_m = \frac{-1}{w_s \cdot (\beta' + K.\alpha.\beta(j\omega))} \tag{12}$$

These methodologies require data for the parasitic capacitance, which can't be obtained from the datasheet [22], as the values are considered inaccurate for high-frequency SORC design. In fact, there are significant differences between the datasheet, SPICE, and experimental capacitance values. To solve this issue, the method from [14] is used: a simple experimental procedure measures the relationship between voltage and current variations to determine a capacitance value used for the command circuit design. An equivalent procedure can be realized for SPICE simulation capacitance measurement.

We've found that the charge and capacitance of switches in the utilized SPICE models differ from those found in practical implementations. Not all SPICE models for switches account for the non-linear variations in gate charge Q_g and capacitance C_{Eq} with the applied V_{ds} voltage. And, for complete models that do consider this non-linearity, extracting the parameters from the SPICE files is not straightforward. However, we can obtain both parameters for a single operating point through the simple introduction of a known gate voltage signal in the model. The gate charge can then be determined using (13).

$$Q_g = \int_{t_0}^{t_1} i_g \, dt \tag{13}$$

From the gate charge Q_g and the applied gate voltage ΔV_g, the total gate capacitance C_{Eq} can be determined using (14).

$$C_{Eq} = \frac{\int_{t_0}^{t_1} i_g \, dt}{\Delta V_g} \tag{14}$$

For the experimental acquisition of these parameters, the chosen nominal voltage and current values in the SORC design should be used, and only the design frequency should be minimized. In this case, the methodology presented in [11] or [18] can be employed because, at low frequencies, the capacitances of the switches do not substantially change the circuit behavior.

[1]The complete equation is too long to be fully developed in here. It was kept the same as in the original reference [15].

IV. Design Methodology Improvement

We have observed, through fiddling with simulation parameters, that increasing the CT's secondary current increased the range of operation. We found that the minimal gate current i_g required for self-sustained oscillation has a linear relationship with operation frequency and that it is proportional to the gate charge value Q_g. Thus, we propose a modification to equation (5) [11], [14], [15], [18], altering the value of the designed secondary current of the CT to consider Q_g and circuit's f_s. The resulting design equation for the secondary current (15) allows self-oscillation in higher frequencies.

$$i_x = \frac{P_z}{V_z} + f_s \cdot \int_{t_0}^{t_1} i_g \, dt = \frac{P_z}{V_z} + f_s \cdot Q_g \qquad (15)$$

It is postulated that, despite the integration of C_{Eq} into the descriptive function for the methodology from [13], since the secondary currents i_x of the current transformer are calculated exclusively based on the voltage ratio of the intended zener diode and its bias current, as the frequency or the MOSFET capacitance increases, the circuit is unable to charge C_{Eq} in time and there is a lack of self-sustained oscillation. Increasing the current provided by the CT would then decrease the charging time.

V. Simulation Results

In this paper, the same design procedures are applied for sequentially increasing frequencies f_r, from 25 kHz up to 1 MHz. The resonance parameters of a LC resonant tank are kept normalized for the entire frequency range, with small deviation when implemented with real components.

Using predetermined f_r frequency values, as well as defined parameters for normalized switching frequency $A = 1.2 f_r$, quality factor $Q = 1.5$, input bus voltage $E = 140\ V$, output power $P_{out} = 50\ W$ and load resistance $R_{out} = 50\ \Omega$, a closest fit routine is applied to the resonant equations presented in section III-A.

We define design parameters $V_z = 16\ V$, $P_z = 0.5\ W$, $i_{load} = 1.1\ A$ and the SPICE model of an IPP220N25NFD MOSFET [23], with gate capacitance $C_g = 5839\ pF$ and gate charge $Q_g = 175\ nC$. This selection of switch, which has unusually high capacitance, is intentional, as it highlights the C_{Eq} effect in the model. Fig. 6 shows the simulation waveforms.

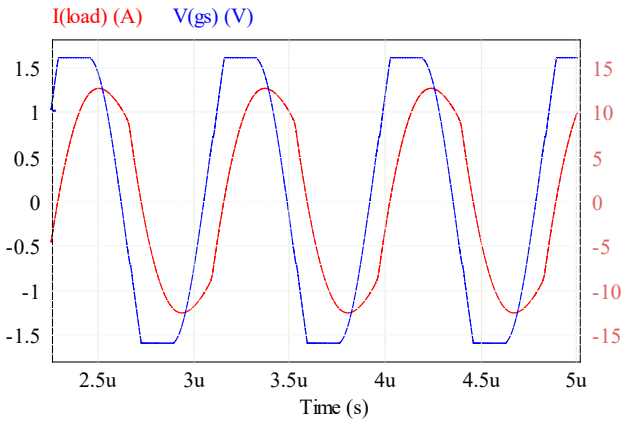

Fig. 6. SPICE simulation load current i_{load} and gate-source voltage V_{gs} for $f_s = 1190\ kHz$.

Table I shows simulation results for different SORC models and methodologies, including the improved one. From the data, it's clear that if MOSFETs with substantial capacitance are utilized in higher frequencies, the methodologies [18] and [15] become unreliable due to lack of current to supply the gate charge. In the case of this specific MOSFET, the effect is noticeable even in the normal design range of the methodologies. For the improved methodology, the turn relationship n effectively is decreased as the frequency rises to compensate charging of the gate capacitance.

VI. Experimental Results

The addition of $f_s \cdot Q_g$ ensures that the current in the secondary side of CT is sufficient to drive the switches. Although this additional variable could have been neglected for switches with low Q_g, experimental tests are used to validate the method using the same MOSFET with high capacitance as the simulation (IPP220N25NFD [23]). The practical capacitance is measured at $6678\ pF$.

Table II shows data obtained through experimental results with the proposed methodology, succeeding to sustain self-oscillation for all the designed resonant filters at a practical switching frequency f_{sp}. These experimental results are then compared to the designed switching frequency $f_s = 1.2/(2\pi\sqrt{L_f C_f})$, calculated from practical component values L_F and C_F that are retroactively considered in the design

TABLE I
Simulation results and No Self-Oscillation (NSO) conditions for different SORC methodologies.

	[18] First Methodology				[14] Second Methodology				Improved Methodology			
$f_r[kHz]$	n	$L_m[\mu H]$	$f_s[kHz]$	$i_{load}[A]$	n	$L'_m[\mu H]$	$f_s[kHz]$	$i_{load}[A]$	n	$L_m[\mu H]$	$f_s[kHz]$	$i_{load}[A]$
25	8.27	1085.00	23.00	1.22	16.54	752.46	31.00	1.00	14.31	687.75	32.00	1.02
50	8.24	517.52	NSO	NSO	16.49	262.36	NSO	NSO	12.46	228.13	64.75	1.04
100	8.36	287.80	NSO	NSO	16.73	98.22	NSO	NSO	10.40	80.14	120.90	1.05
250	8.29	108.15	NSO	NSO	16.59	19.93	NSO	NSO	6.44	14.84	306.00	1.06
500	8.32	55.24	NSO	NSO	16.64	5.73	NSO	NSO	4.04	4.10	605.00	1.05
1000	8.36	28.78	NSO	NSO	16.73	1.60	NSO	NSO	2.36	1.12	1190.00	1.02

TABLE II
EXPERIMENTAL RESULTS FOR DESIGNED FILTERS.

$L_F[\mu H]$	$C_F[nF]$	$f_r[kHz]$	$f_s[kHz]$	$f_{sp}[kHz]$	$i_{load}[A]$
481.20	79.48	25.74	30.88	30.35	0.86
237.40	40.93	51.06	61.27	60.26	0.96
111.50	21.91	101.83	122.19	121.40	0.89
53.90	8.12	240.57	288.69	306.90	0.70
25.59	4.22	484.32	581.18	548.90	0.78
11.94	2.81	869.00	1042.80	1050.00	0.71

procedure. For all frequencies, the reference i_{load} current is 1 A. Both the frequency and current discrepancies from designed values are within reason and an there is a noticeable improvement over methodologies [14] and [18], even as the design frequency deviation increases as the frequency increases. Fig. 7 shows the practical current waveforms for the 1 MHz design.

A. Resistive Load Model Considerations

Lighting sources, such as Fluorescent Lamps and, particularly LEDs, characteristically are subject to temperature variations that cause changes to their electrical characteristics, being highly non-linear. However, by maintaining a fixed equivalent value for the resistive load during the design of the SORC, we ensure that we are operating under the assumption that the lighting source is functioning at a very specific point of non-varying electrical characteristics. This approach effectively eliminates any potential errors from the filter design stage that could impact subsequent steps in the SORC design methodology.

Therefore, the use of a resistive load in the experimental setup when testing a new methodology for the SORC is acceptable in the first steps of its development. For one, the SORC design requires, as a previous step, the analysis of the resonant filter, which incorporates the electrical characteristics of the lighting source.

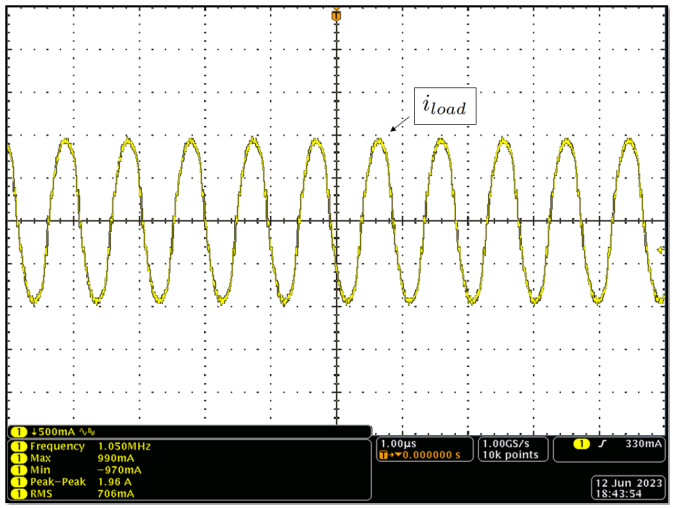

Fig. 7. Experimental load current i_{load} at f_s = 1050 kHz. Vertical Scale: 500 mA/div Horizontal Scale: 1 µs/div.

B. Zero Voltage Switching Considerations

ZVS is essential for high-efficiency operation, especially at higher frequencies. It is commonly assumed that ZVS margins are guaranteed by operating at a switching frequency above the resonance frequency. However, in this paper, we observed that As the designed switching frequencies increased, the ZVS margins progressively diminished until the ZVS condition was no longer attainable beyond 500 kHz. This phenomenon was accompanied by a progressive increase in the phase shift between the primary and secondary currents of the CT - therefore, we hypothesize this is partly due to the presence of significant MOSFET gate capacitance C_{Eq} at the secondary.

Intentionally using a MOSFET with substantial gate capacitance accentuated the significance of Q_g and helped formulate (15). However, as ZVS conditions are traditionally determined without considering gate capacitance, we seek to address this effect in future research, investigating design parameter adjustments or circuit modifications to restore ZVS. This will be a key focus of our forthcoming work.

VII. CONCLUSION

This paper evaluates two SORC design methodologies at frequencies higher than their original design range and adds a modification to the methodology from [14] and [18], successfully enabling the design methodolgoy for higher frequencies or higher MOSFET gate capacitances. Practical implementations are functional, but have revealed a noticeable increase in phase shift between primary and secondary currents as the switching frequency rises. This phase shift significantly influences ZVS conditions and is believed to be partially caused by the MOSFETs gate capacitance. Future research efforts will be directed at exploring design parameters and circuit adjustments required to mitigate this phase shift. Following papers should include tests in even higher frequencies and with other switch technologies (e.g. GaNFET), contributing to the wider adoption of SORCs for lighting.

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